DATA SHEET

TDA4670
Picture Signal Improvement (PSI) circuit

Product specification
Supersedes data of May 1991
File under Integrated Circuits, IC02

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Philips Semiconductors

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FEATURES

- Luminance signal delay from 20 to 1100 ns (minimum step 45 ns)
- Luminance signal peaking with selectable symmetrical overshoots
- 2.6 or 5 MHz peaking centre frequency and selectable degree of peaking (–3, 0, +3 and +6 dB)
- Selectable noise reduction by coring
- Handles negative and positive colour-difference signals
- Selectable Colour Transient Improvement (CTI) to decrease the colour-difference signal transient times to those of the high frequency luminance signals
- Selectable 5 or 12 V sandcastle input voltage
- All controls selected via the I^2C-bus
- Timing pulse generation for clamping and delay time control synchronized by sandcastle pulse
- Automatic luminance signal delay correction using a control loop
- Luminance and colour-difference input signal clamping with coupling capacitor
- 4.5 to 8.8 V supply voltage range
- Minimum of external components required.

GENERAL DESCRIPTION

The TDA4670 delays the luminance signal and improves colour-difference signal transients. Additionally, the luminance signal can be improved by peaking and noise reduction (coring).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 1 and 5)	4.5	5	8.8	V
$I_{P(tot)}$	total supply current	31	41	52	mA
$t_{d(Y)}$	Y signal delay time	20	–	1130	ns
$V_{i(VBS)}$	composite Y input signal (peak-to-peak value, pin 16)	–	450	640	mV
$V_{i(CD)(p\text{-}p)}$	colour-difference input signal (peak-to-peak value)				
	±(R – Y) on pin 3	–	1.05	1.48	V
	±(R – Y) on pin 7	–	1.33	1.88	V
G_Y	gain of Y channel	–	–1	–	dB
G_{CD}	gain of colour-difference channel	–	0	–	dB
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4670	DIP18	plastic dual in-line package; 18 leads (300 mil)	SOT102-1

BLOCK DIAGRAM

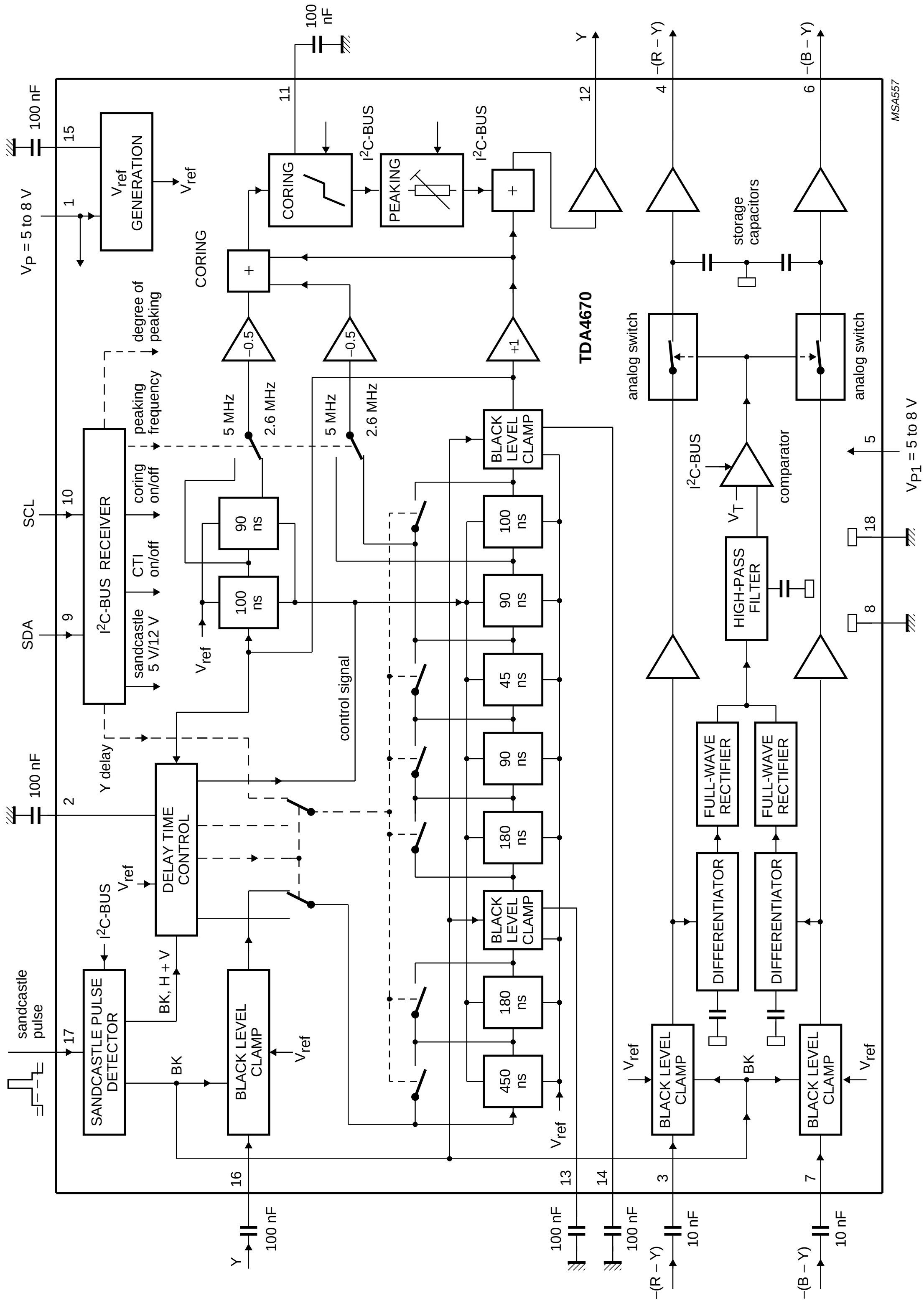


Fig.1 Block diagram.

Picture Signal Improvement (PSI) circuit TDA4670

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
C_{DL}	2	capacitor of delay time control
$V_{i(R-Y)}$	3	±(R – Y) colour-difference input signal
$V_{o(R-Y)}$	4	±(R – Y) colour-difference output signal
V_{P2}	5	positive supply voltage 2
$V_{o(B-Y)}$	6	±(B – Y) colour-difference output signal
$V_{i(B-Y)}$	7	±(B – Y) colour-difference input signal
GND2	8	ground 2 (0 V)
SDA	9	I^2C-bus serial data input/output
SCL	10	I^2C-bus serial clock input
C_{COR}	11	coring capacitor
V_{oY}	12	delayed luminance output signal
C_{CLP1}	13	black level clamping capacitor 1
C_{CLP2}	14	black level clamping capacitor 2
C_{ref}	15	capacitor of reference voltage
V_{iY}	16	luminance input signal
SAND	17	sandcastle pulse input
GND1	18	ground 1 (0 V)

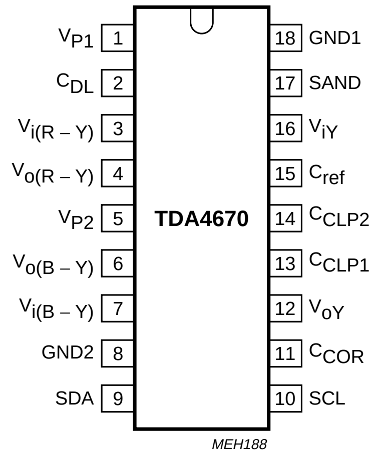


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4670 contains luminance signal processing and colour-difference signal processing. The luminance signal section comprises a variable integrated luminance delay line with luminance signal peaking and noise reduction by coring.

The colour-difference section consists of a transient improvement circuit to decrease the rise and fall times of the colour-difference signal transients. All functions and parameters are controlled via the I^{2}C-bus.

Y-signal path

The video and blanking signal is AC-coupled to the input at pin 16. Its black porch is clamped to a DC reference voltage to ensure the correct operating range of the luminance delay stage.

The luminance delay line consists of all-pass filter sections with delay times of 45, 90, 100, 180 and 450 ns (see Fig.1). The luminance signal delay is controlled via the I^{2}C-bus in steps of 45 ns in the range of 20 to 1100 ns, this ensures that the maximum delay difference between the luminance and colour-difference signals is ±22.5 ns.

An automatic luminance delay time adjustment in an internal control loop (with the horizontal frequency as a reference) is used to correct changes in the delay time, due to component tolerances. The control loop is automatically enabled between the burst key pulses of lines 16 (330) and 17 (331) during the vertical blanking interval. The control voltage is stored in the capacitor C_{DL} connected to pin 2.

The peaking section uses a transversal filter circuit with selectable centre frequencies of 2.6 and 5 MHz.

It provides selectable degrees of peaking of –3, 0, +3 and +6 dB and a noise reduction by coring, which attenuates the high-frequency noise introduced by peaking.

The output buffer stage ensures a low-ohmic VBS output signal on pin 12 (<160 Ω). The gain of the luminance signal path from pin 16 to pin 12 is unity.

An oscillation signal of the delay time control loop is present on output pin 12 instead of the VBS signal during the vertical blanking interval in lines 16 (330) to 18 (332). Therefore, this output signal should not be applied for synchronization.

Colour-difference signal paths

The colour-difference input signals (on pins 3 and 7) are clamped to a reference voltage.

Each colour-difference signal is fed to a transient detector and to an analog signal switch with an attached voltage storage stage.

The transient detectors consist of differentiators and full-wave rectifiers. The output voltages of both transient detectors are added and then compared in a comparator. This comparator controls both following analog signal switches simultaneously.

The analog signal switches are in an open position at a certain value of transient time; the held value (held by storage capacitors) is then applied to the outputs.
The switches close to rapidly accept the actual signal levels at the end of these transients. The improved transient time is approximately 100 ns long and independent of the input signal transient time.

Colour-difference paths are independent of the input signal polarity and have a gain of unity.

The CTI functions are switched on and off via the I^{2}C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). V_{P1} and V_{P2} as well as GND1 and GND2 connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 1)		0	8.8	V
V_{P2}	supply voltage (pin 5)		0	8.8	V
P_{tot}	total power dissipation		0	0.97	W
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
V_{ESD}	electrostatic handling	note 1			
	for pins 9 and 10		–	+300	V
			–	–500	V
	for other pins		–	±500	V

Note

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	82	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; nominal video amplitude $V_{VB} = 315$ mV; $t_H = 64$ µs; $t_{BK} = 4$ µs (burst key); $T_{amb} = 25$ °C; measurements taken in Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 1)		4.5	5	8.8	V
V_{P2}	supply voltage (pin 5)		4.5	5	8.8	V
$I_{P(tot)}$	total supply current		31	41	52	mA
Y-signal path						
$V_{i(Y)(p\text{-}p)}$	VBS input signal on pin 16 (peak-to-peak value)		–	450	640	mV
V_{16}	black level clamping voltage		–	3.1	–	V
I_{16}	input current	during clamping	±95	–	±190	µA
		outside clamping	–	–	±0.1	µA
R_{16}	input resistance	outside clamping	5	–	–	MΩ
C_{16}	input capacitance		–	3	10	pF
$t_{d(Y)(max)}$	maximum Y delay time	set via I^2C-bus	1070	1100	1130	ns
$t_{d(Y)(min)}$	minimum Y delay time	set via I^2C-bus	–	20	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta t_{d(Y)}$	minimum delay step	set via I^2C-bus	40	45	50	ns
	group delay time difference	f = 0.5 to 5 MHz; maximum delay	–	0	±25	ns
	delay time difference between Y and colour-difference signals	Y delay; CTI and peaking off	70	100	130	ns
$t_{d(peak)(min)}$	minimum delay time for peaking		185	215	245	ns
G_Y	VBS signal gain measured on output pin 12 (composite signal, peak-to-peak value)	V_o/V_i; f = 500 kHz; maximum delay	–2	–1	0	dB
I_{12}	output current (emitter-follower with constant current source)	source current	–1	–	–	mA
		sink current	0.4	–	–	mA
R_{12}	output resistance		–	–	160	Ω
f_{res}	frequency response for	maximum delay				
		f = 0.5 to 3 MHz	–2	–1	0	dB
		f = 0.5 to 5 MHz	–4	–3	–1	dB
LIN	signal linearity for	$\alpha_{min}/\alpha_{max}$;				
	video contents of 315 mV (p-p)	V_{VBS} = 450 mV (p-p)	0.85	–	–	–
	video contents of 450 mV (p-p)	V_{VBS} = 640 mV (p-p)	0.60	–	–	–
Luminance peaking, selected via I^2C-bus						
f_{peak}	peaking frequency	f_{C1}; LCF-bit = 0	4.5	5	5.5	MHz
		f_{C2}; LCF-bit = 1	2.3	2.6	2.9	MHz
V_{peak}	peaking amplitude for grade of peaking (f_C amplitude/0.5 MHz amplitude)					
	selectable values		–	–3	–	dB
			–	0	–	dB
			–	+3	–	dB
			–	+6	–	dB
	limitation of peaking (positive amplitude of correction signal referenced to 315 mV)		–	20	–	%
$V_{n(rms)}$	noise voltage on pin 12 (RMS value)	without peaking; f = 0 to 5 MHz	–	–	1	mV
COR	coring of peaking (coring part referenced to 315 mV)	COR-bit = 1	–	20	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Colour-difference paths measured with transient times $t_r = t_f = 1$ µs; $t_{p\,H} \geq 1$ µs; $V_i = 1.33$ V (p-p) on pins 3 and 7 and with burst key pulse $t_{BK} = 4$ µs						
$V_{i(CD)(p-p)}$	±(R – Y) input signal (peak-to-peak value; pin 3)	75% colour bar	–	1.05	1.48	V
	±(B – Y) input signal (peak-to-peak value; pin 7)	75% colour bar	–	1.33	1.88	V
	input transient sensitivity	$V_{3,7}/\delta t$	0.15	–	–	V/µs
$V_{3,7}$	internal clamping voltage level		–	2.45	–	V
$I_{3,7}$	input current	outside clamping	–	–	±1	µA
		during clamping	±100	–	±190	µA
$C_{3,7}$	input capacitance		–	6	12	pF
$V_{4,6}$	DC output voltage		–	2	–	V
$\Delta V_{4,6}$	output offset voltage	$R_S \leq 300\ \Omega$; note 1	–	–	±5	mV
		during and after storage time	–	–	±18	mV
V_{spike}	spurious spike signals on pins 4 and 6	$R_S \leq 300\ \Omega$; note 1	–	–	±30	mV
$I_{4,6}$	output current (emitter-follower with constant current source)	source current	–1	–	–	mA
		sink current	0.4	–	–	mA
$R_{4,6}$	output resistance		–	–	100	Ω
G_v	signal gain in each path	V_o/V_i	–1	0	+1	dB
ΔG_v	gain difference –(R – Y)/–(B – Y)		–	0	±0.3	dB
LIN	signal linearity for	$\alpha_{min}/\alpha_{max}$;				
	nominal signal	$V_i = 1.33$ V (p-p)	0.90	–	–	–
	+3 dB signal	$V_i = 1.88$ V (p-p)	0.65	–	–	–
ΔV_o	signal reduction at higher frequency (output signal ratio V_i/V_o)	signal with $t_{p\,H} = 50$ ns; $t_r = t_f = 1$ µs	–1.5	–	–	dB
Sandcastle pulse, input voltage selectable via I²C-bus						
V_{17}	input voltage threshold for H and V sync	SC5-bit = 0 (+12 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 0 (+12 V)	5.5	6.5	7.5	V
	input voltage threshold for H and V sync	SC5-bit = 1 (+5 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 1 (+5 V)	3.0	3.5	4.0	V
R_{17}	input resistance	+12 V input level	30	40	50	kΩ
		+5 V input level	15	20	25	kΩ
C_{17}	input capacitance		–	4	8	pF
t_{BK}	burst key pulse width		3.0	4.0	4.6	µs
t_d	leading edge delay for clamping pulse	referenced to t_{BK}	–	1	–	µs
n_p	number of required burst key pulses vertical blanking interval	note 2	4	–	31	–

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus control, SDA and SCL						
V_{IH}	HIGH level input voltage on pins 9 and 10		3	–	5	V
V_{IL}	LOW level input voltage		0	–	1.5	V
$I_{9,10}$	input current		–	–	±10	μA
$V_{o(ACK)}$	output voltage at acknowledge on pin 9	$I_{o(ACK)}$ = 3 mA	–	–	0.4	V
$I_{o(ACK)}$	output current at acknowledge on pin 9	sink current	3	–	–	mA

Notes

1. Crosstalk on output, measured in the unused channel when the other channel is provided with a nominal input signal (CTI active).
2. A number of more than 31 burst key pulses repeats the counter cycle of delay time control.

I^2C-BUS FORMAT

S(1)	SLAVE ADDRESS(2)	ACK(3)	SUBADDRESS(4)	ACK(3)	DATA(5)	P(6)

Notes

1. S = START condition.
2. SLAVE ADDRESS = 1000 100X.
3. ACK = acknowledge, generated by the slave.
4. SUBADDRESS = subaddress byte, see Table 1.
5. DATA = data byte, see Table 1.
6. P = STOP condition.
7. X = read/write control bit.

   X = 0, to write (the circuit is slave receiver only).

If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I^2C-bus transmission; see Table 2

FUNCTION	SUBADDRESS	DATA							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Y delay/CTI/SC	00010000	0	SC5	CTI	DL4	DL3	DL2	DL1	DL0
Peaking and coring	00010001	COR	PEAK	LCF	0	0	0	PCON1	PCON0

Table 2 Function of the bits

DATA	FUNCTION	LOGIC 1	LOGIC 0
DL0	set delay in luminance channel	45 ns	0 ns
DL1		90 ns	0 ns
DL2		180 ns	0 ns
DL3		180 ns	0 ns
DL4		450 ns	0 ns
CTI	set colour transient improvement	active	inactive
SC5	select sandcastle pulse voltage	+5 V	+12 V
LCF	set peaking frequency response	2.6 MHz	5.0 MHz
PEAK	set peaking delay	active	inactive
COR	set coring control	active	inactive
PCONx	set peaking amplification	see Table 3	

Table 3 Peaking amplification

PCON1	PCON0	GRADE OF PEAKING (dB)
0	0	–3
0	1	0
1	0	+3
1	1	+6

Remarks to the subaddress bytes

Subaddresses 00H to 0FH are reserved for colour decoders and RGB processors.

Subaddresses 10 and 11 only are acknowledged.

General call address is not acknowledged.

Power-on-reset: D7 to D1 bits of data bytes are set to logic 0, D0 bit is set to logic 1.

INTERNAL CIRCUITRY

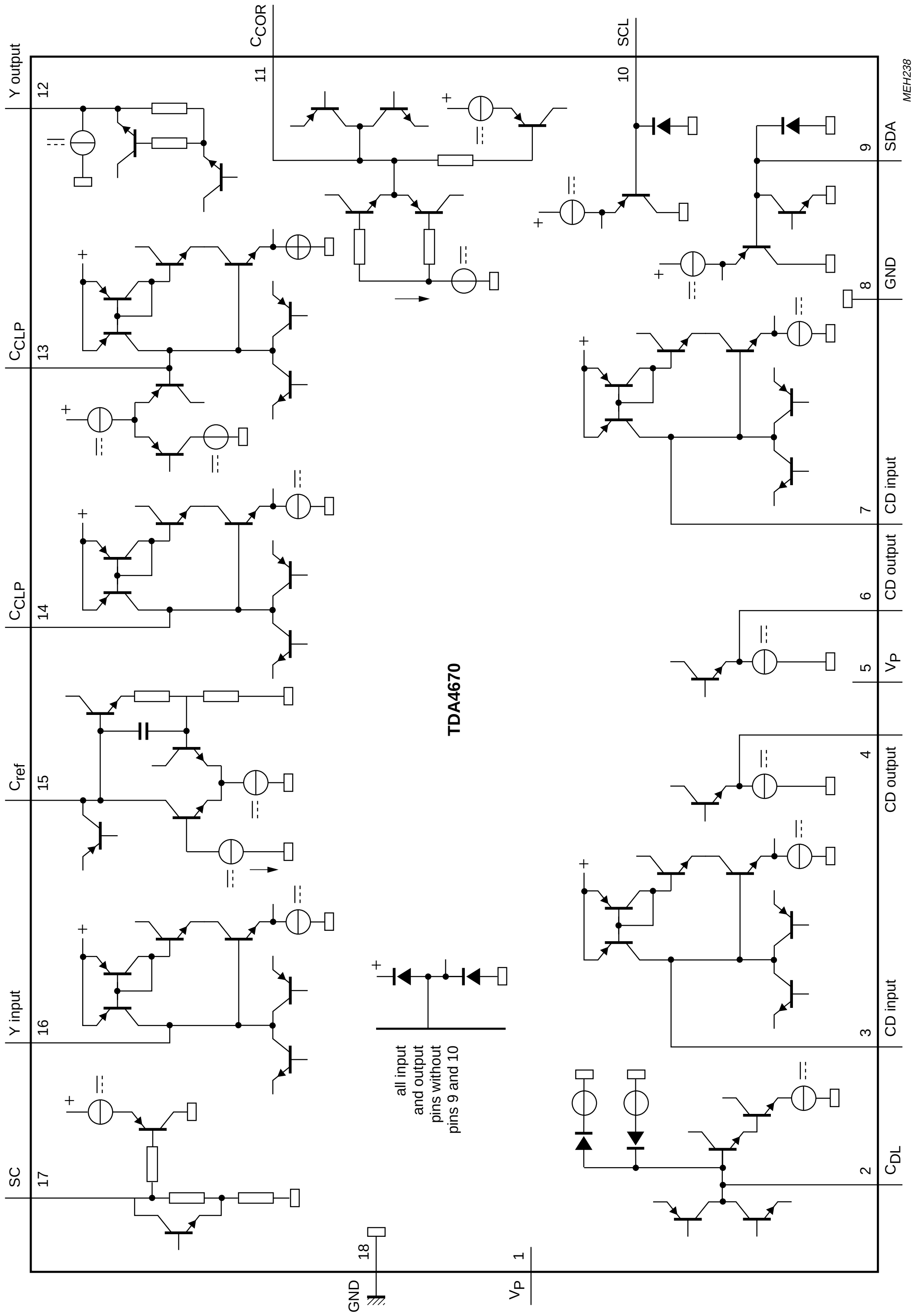


Fig.3 Internal circuit.

TEST AND APPLICATION INFORMATION

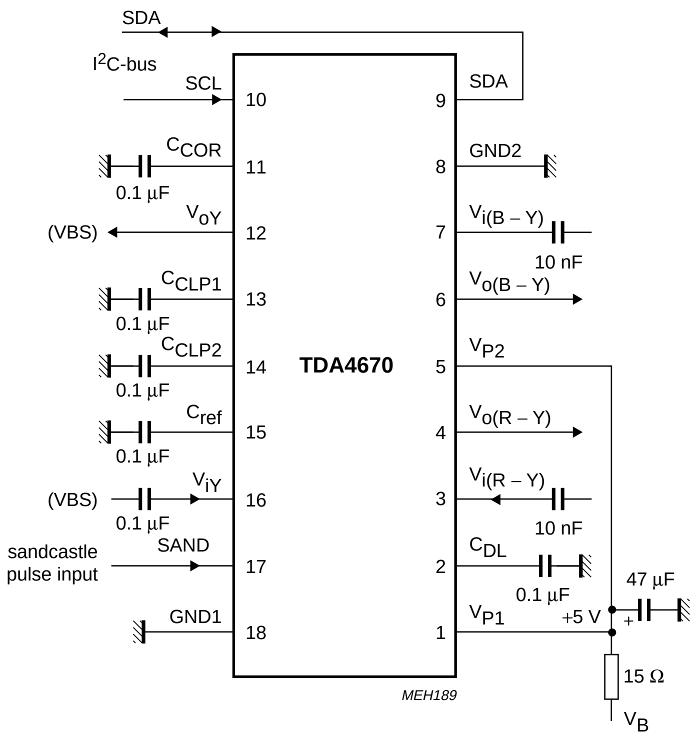
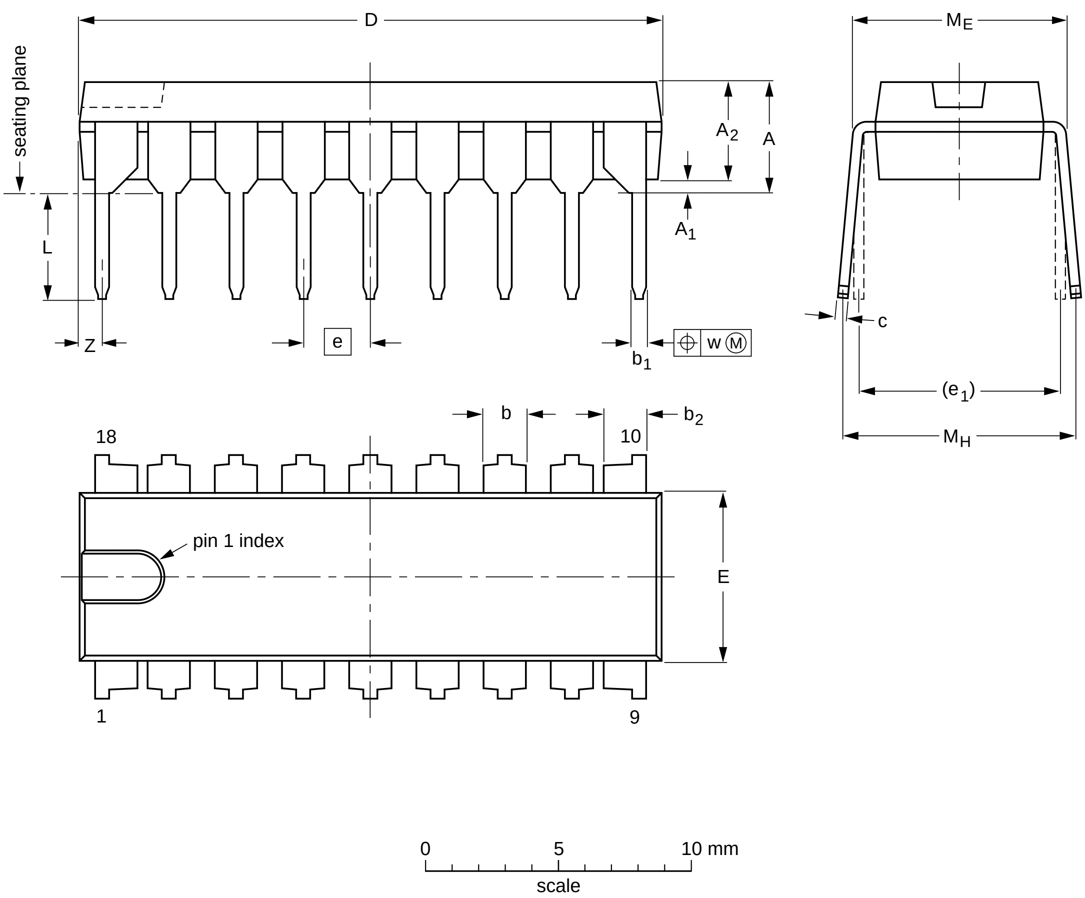


Fig.4 Test and application circuit.

PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds.
The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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